Amendments to the Claims:

Claims 2, 3, 14, and 15 have been cancelled. Claims 1, 4-6, 8, 11, 13, 17, 21, 23, and 25 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A dynamic random access memory device (DRAM), comprising:

at least one memory bank;

control logic associated with the at least one memory bank to control data corresponding to a memory command within the DRAM; and

a FIFO associated with the control logic, the FIFO configured for temporarily storing at least one ~~a~~ memory command until at least one of the data corresponding to the at least one memory command arrives at the DRAM, the at least one memory command including an address within the at least one memory, the control logic further configured for simultaneous reading and writing from the FIFO, the control logic further including [[a]] at least one read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter during a current reading from the FIFO.

2. (Cancelled).

3. (Cancelled).

4. (Currently Amended) The DRAM of claim 1[[3]], further comprising at least one write counter associated with the FIFO.

5. (Currently Amended) The DRAM of claim 1[[3]], wherein the at least one register is a linear feedback shift register.

6. (Currently Amended) A FIFO buffer system in a dynamic random access memory device (DRAM), comprising:

a FIFO configured for temporarily storing at least one memory command until at least one data corresponding to the at least one memory command arrives at the DRAM;

at least one write counter associated with the FIFO; and

at least one read counter associated with the FIFO, the at least one read counter comprising at least one pointer register configured to maintain a previous read counter setting of the at least one read counter during a current reading from the FIFO.

7. (Original) The FIFO buffer system of claim 6, wherein the at least one pointer register is a linear feedback shift register.

8. (Currently Amended) An electronic system, comprising:

a processor;

at least one of an input device, an output device and a storage device associated with the processor; and

a memory device coupled to the processor for storing data and instructions for use by the processor, the memory device comprising:

at least one FIFO configured for temporarily storing at least one of the instructions until at least one of the data corresponding to the at least one of the instructions arrives at the memory device;

at least one write counter associated with the at least one FIFO; and

at least one read counter associated with the at least one FIFO, the at least one read counter comprising at least one pointer register configured to maintain a previous read counter setting of the at least one read counter during a current reading from the FIFO.

9. (Original) The electronic system of claim 8, wherein the memory device is a DRAM.

10. (Original) The electronic system of claim 8, wherein the electronic system comprises at least one each of an input device, an output device and a storage device.

11. (Currently Amended) A semiconductor substrate including a FIFO buffer, comprising:

at least one FIFO;

at least one write counter associated with the at least one FIFO; and

at least one read counter associated with the at least one FIFO, the at least one read counter comprising at least one pointer register configured to maintain a previous read counter setting of the at least one read counter during a current reading from the FIFO.

12. (Original) The semiconductor substrate of claim 11, wherein the semiconductor substrate is a semiconductor wafer.

13. (Currently Amended) A semiconductor substrate including a DRAM, comprising:

at least one memory bank;

control logic associated with the at least one memory bank to control at least one of data and commands within the DRAM; and

a FIFO associated with the control logic, the FIFO configured for temporarily storing a memory command until data corresponding to the memory command arrives at the DRAM, the control logic further configured for simultaneous reading and writing of the at least one of data and commands from the FIFO, the control logic further including at least one [[a]] read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter during a current reading from the FIFO.

14. (Cancelled).

15. (Cancelled).

16. (Original) The semiconductor substrate of claim 13, wherein the semiconductor substrate is a semiconductor wafer.

17. (Currently Amended) A method of storing data in a DRAM, comprising:

providing a DRAM comprising at least one memory bank, control logic associated with the at least one memory bank, and a FIFO associated with the control logic, the FIFO configured for temporarily storing a memory bank address command until data corresponding to the memory bank address command arrives at the DRAM, the at least one memory command specifying addressing within the at least one memory bank, the control logic configured for simultaneous reading and writing from the FIFO, the control logic further including a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter during a current reading from the FIFO;

receiving the memory bank address command at the control logic;

writing the memory bank address command to the FIFO;

receiving data corresponding to the memory bank address command at the control logic;

reading the memory bank address command from the FIFO; and

storing the data at a memory bank address indicated by the memory bank address command.

18. (Original) The method of claim 17, further comprising:
providing a write counter associated with the FIFO and pointing at a first buffer of the FIFO;
transmitting a first write latch signal through a write latch input to the write counter; and
adjusting the write counter to point at a second buffer of the FIFO in response to the first write latch signal.

19. (Original) The method of claim 18, further comprising transmitting a reset signal through a reset input to the write counter prior to transmitting the first write latch signal.

20. (Original) The method of claim 18, wherein the memory bank address command is a first memory bank address command written to the first buffer of the FIFO, the method further comprising:
receiving a second memory bank address command at the control logic;
receiving data corresponding to the second memory bank address command at the control logic; and
reading the second memory bank address command from the second buffer of the FIFO.

21. (Currently Amended) The method of claim 17, wherein the FIFO comprises a sequential plurality of FIFO buffers, the method further comprising:
providing ~~a read counter and~~ a write counter, the read counter and the write counter each pointing at a different one of the sequential plurality of FIFO buffers; and
maintaining the write counter for pointing to at least one FIFO buffer ahead in the sequential plurality of FIFO buffers to which the read counter is pointing.

22. (Original) The method of claim 21, further comprising receiving at least one write latch signal through a write latch input to the write counter prior to providing the read counter and the write counter, each pointing at a different one of the sequential plurality of FIFO buffers.

23. (Currently Amended) A method of buffering a data stream including a memory bank address command and data corresponding to the memory bank address command in an electronic device, the method comprising:

providing a FIFO buffer system having a read counter pointing at a first buffer of a FIFO including a series of FIFO buffers and a write counter pointing at the first buffer of the FIFO, the FIFO buffers configured for temporarily storing the memory bank address command while retrieving the data corresponding to the memory bank address command;

receiving the memory bank address command of the data stream at the FIFO buffer system;

storing the memory bank address command of the data stream in the first buffer of the FIFO;

adjusting the write counter to point at a second buffer in the series of FIFO buffers; and

maintaining the write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of the first buffer at which the read counter is pointing and maintaining a read counter pointing to at least one FIFO buffer associated with a previous read counter setting during a current reading from the FIFO.

24. (Original) The method of claim 23, further comprising extracting the memory bank address command of the data stream from the first buffer in response to a read command transmitted to the FIFO buffer system from a controller associated with the data stream and the FIFO buffer system.

25. (Currently Amended) A method of operating a memory device, the method comprising:

receiving at least one memory bank address command;

temporarily storing in a FIFO a first of the at least one memory bank address command, the FIFO including a series of FIFO buffers;

temporarily storing in the FIFO a second of the at least one memory bank address command;

receiving data corresponding to the first of the at least one memory bank address command;

storing in the FIFO the data corresponding to the first of the at least one memory bank address command in response to the first of the at least one memory bank address command;

receiving data corresponding to the second of the at least one memory bank address command;

storing in the FIFO the data corresponding to the second of the at least one memory bank address command; and

maintaining <u>a</u> ~~the~~ write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of <u>a</u> ~~the~~ first <u>FIFO</u> buffer at which <u>a</u> ~~the~~ read counter is pointing and maintaining <u>the</u> [[a]] read counter pointing to at least <u>another</u> ~~one~~ FIFO buffer associated with a previous read counter setting <u>during a current reading from the FIFO</u>.